ABSTRACT

A nonvolatile semiconductor memory device includes a plurality of memory transistors, a plurality of insulating layers disposed over the transistors, and a plurality of metal layers. Each of the metal layers is disposed on one of the insulating layers. The device also includes a plurality of metal plugs disposed over corresponding memory transistors. Each of the metal plugs filling in a contact hole formed in one of the insulating layers and electrically connecting the metal layers disposed on a top side and a bottom side of the corresponding insulating layer. A top metal layer of the plurality of metal layers is configured to provide bit lines that correspond to the memory transistors, the metal plugs are vertically aligned, and one of the insulating layers is configured so that whether one of the memory transistors is connected to a corresponding bit line is determined by whether a metal plug corresponding to the memory transistor exists in the insulating layer.